REMARKS

Reconsideration and allowance of the above-referenced application are respectfully requested.

Claim 8 stands objected to due to informalities. In response, the specific issue noted by the Examiner has been complied with herein.

Claims 1, 2, 4-8, 17 and 18 stand rejected under 35 USC 102(b) as being anticipated by Garibay. Initially, the rejection of these claims refers to the phrase in claim 17 of "adapted to", and alleges that this only requires the ability to perform a function but does not constitute a limitation. In order to obviate this rejection, claim 17 has been amended to recite that the control unit operates to issue the instruction and at least part of the status information in parallel. This obviates the alleged issue of whether "adapted to" is a positive limitation or not. However, Applicant reserves the right to show that the Patent Office's legal interpretation of "adapted to" is not correct.

It is respectfully suggested that nothing in Garibay issues the instruction and status information in parallel, where the

status information word has bits that represent multiple different kinds of exceptions as claimed.

In responding to Applicant's previous comments about claim 1, the rejection states that Garibay discloses a plurality of different exception conditions, and that "digitally speaking, it is clearly inherent that a plurality of exception conditions can only be represented by a set of bits". It is respectfully suggested that this argument is based on a healthy amount of hindsight. Clearly, Garibay states that there can be any of a selected number of exception conditions. However, the present claim 1 defines that there is an exception status information word with bits that represent the multiple kinds of exceptions. This is almost the antithesis of what is stated in Garibay. The Garibay abstract states that if the unit detects any of the exception conditions, it invalidates the instruction by clearing the single validity bit. That is, according to the abstract, all of the different kinds of exceptions are all represented by the same single bit action: that is, clearing the valid bit (see, for example, column 4, lines 44-59). As stated above, this is absolutely the antithesis of what is done and claimed by claim 1; which specifies a multiple bit exception word, having bits that represent multiple different kinds of exceptions.

The rejection also refers to claim 1 which again refers to the valid bit which is either set or reset based on different exceptions. Admittedly these can be multiple different kinds of different exceptions. Again, each of these different exceptions change the value of a single bit: not the state of bits of the multiple bit exception word representing multiple different kinds of exceptions, as claimed.

The entire disclosure is entirely consistent with this teaching. Specifically, column 4, lines 24-30, specify that "any of the selected number of exception conditions applies..., it invalidates that instruction by clearing the valid bit". That is, for any of the multiple different exceptions, a single bit is cleared. No attempt is made to use different bits to differentiate between the different kinds of exceptions. Therefore, there is no teaching or suggestion that the state of bits of said multiple bit exception word representing multiple different kinds of exceptions. In fact, Garibay teaches something very different and, in fact, teaches away from this subject matter.

With regard to the statement in the Official Action that it is "inherent", it is respectfully suggested that this is clearly not inherent, since Garibay clearly states that he uses a single

bit to represent each of the different kinds of exceptions, not multiple bits to represent the multiple different kinds of exceptions. Garibay is an entirely different kind of system than the presently claimed system. Therefore claim 1, should be allowable for these reasons, along with the claims which depend therefrom. Specifically, for example, claim 6 specifies generating information that a particular exception condition was not generated. Nothing in Garibay teaches or suggests this feature. Claim 7 specifies detecting the rest of the data block prior to issuing an instruction, which again is not taught or suggested by the cited prior art.

Claim 17 should be allowable for similar reasons; and specifically since the core control unit generates exception status information about the data block which is a multiple bit exception status information word and has states of the multiple bits representing multiple different kinds of exceptions. As described above, this is in no way taught or suggested by the cited prior art.

Claim 18 specifies fetching another data block which again is nowhere taught or suggested by Garibay. While Garibay must be able to obtain multiple data blocks, there is no teaching or suggestion that Garibay stores them both, as claimed.

Therefore, this claim should also be allowable along with the claims which depend therefrom.

Claims 3 and 20 stand rejected as allegedly being obvious over Garibay. The rejection states that Garibay does not disclose the use of an OR gate, but that it would be obvious to use one. The undersigned takes no issue with the bald fact that an OR gate may be used in programmable logic, however, there is no teaching or suggestion that the exception status information, which is a multiple bit exception status information word, is passed through the OR gate to the exception handling logic. While OR gates are known, they are certainly not known for receiving multiple bit exception words representing different kinds of exceptions as claimed.

Claims 10 and 13-16 have been canceled in order to obviate the rejections thereto.

Responding once again to the response to Applicant's previous arguments; Applicant did not intend to say that Garibay discloses only one exception condition; but Applicant did and does contend that Garibay teaches only one single bit, to represent each of the multiple different kinds of exception conditions which can be found. It is certainly not inherent that a plurality of exception conditions can be represented by a

set of bits. Rather, Garibay teaches that the plurality of exception conditions are each represented by one single bit.

It is believed that all of the pending claims have been addressed in this paper. However, failure to address a specific rejection, issue or comment, does not signify agreement with or concession of that rejection, issue or comment. In addition, because the arguments made above are not intended to be exhaustive, there may be reasons for patentability of any or all pending claims (or other claims) that have not been expressed. Finally, nothing in this paper should be construed as an intent to concede any issue with regard to any claim, except as specifically stated in this paper, and the amendment of any claim does not necessarily signify concession of unpatentability of the claim prior to its amendment.

In view of the above amendments and remarks, therefore, all of the claims should be in condition for allowance. A formal notice to that effect is respectfully solicited.

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Please apply any other charges or credits to Deposit Account No. 06-1050.

Respectfully submitted,

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Scott C. Harris
Reg. No. 32,030

Fish & Richardson P.C.
PTO Customer Number: 20985
4350 La Jolla Village Drive, Suite 500
San Diego, CA 92122
Telephone: (858) 678-5070
Facsimile: (858) 678-5099
10378896.doc